Subject Name: LINEAR IC APPLICATIONS

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Year and Sem, Department:II & I SEM, ECE

Unit-I: Integrated Circuits:

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

1. An Integrated circuit is a miniature ,low cost electronic circuit fabricated on a single crystal chip of silicon.
2. IC may be linear or digital.
3. Input offset voltage: Input offset voltage Vio is the differential input voltage that exists between two input terminals of an op-amp without any external inputs applied.
4. Thermal Drift: – The average rate of change of input offset voltage per unit change in temperature is called thermal voltage drift, and is denoted by $\Delta Vio/\Delta T$. Units – $\mu V/°C$
5. The change in op-amp's input offset voltage caused by variations in the supply voltages is called Supply voltage Rejection Ratio or Power Supply Rejection Ratio.
6. Common Mode Rejection Ratio (CMRR): It can be defined as the ratio of the differential gain A_D to the common mode gain A_{cm}, that is CMRR = Ad/Acm
7. DC Characteristics include input bias current, input offset current, Input offset voltage, Output offset voltage and Thermal drift.
8. AC Characteristics include i) Frequency Response ii) Slew Rate.
9. Ideally an op-amp should have an infinite band width.
10. The practical op-amp gain, however, decreases at higher frequencies.
11. The slew rate is defined as the maximum rate of change of output voltage per unit of time and is expressed in volts per micro seconds. In equation form, SR = (dVo/dt)|maximum V/μs.
12. The Differential Amplifier: The open loop differential amplifier in which input signals vin1 and vin2 are applied to the positive and negative input terminals. Since the OPAMP amplifies the difference the between the two input signals, this configuration is called the differential amplifier.
13. The Inverting Amplifier: If the input is applied to only inverting terminal and noninverting terminal is grounded then it is called inverting amplifier.
14. The Non Inverting Amplifier: If the input is applied to only noninverting terminal and inverting terminal is grounded then it is called Noninverting amplifier.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Why Integrated circuits are needed? (March 2016)
2. List all ideal characteristics of Op-amp. (March 2016)
3. What is the effect of negative feedback in non-inverting amplifier? ? (March 2016)
4. Define Linear and Digital ICs. (March 2017)
5. Classify the ICs. (March 2017)
6. Define CMRR. (March 2017)
7. Discuss the following: input bias current, input off set current and thermal drift. (November – 2015)
8. Mention the reasons why open loop is not preferred for linear applications. (Nov/Dec 2017)
9. Define Monolithic and Hybrid IC Technologies. (Nov/Dec 2018)
10. What are the advantages of ICs over discrete circuits? (Nov/Dec 2018)
11. Discuss how a logic buffer amplifier is different from an audio amplifier. (Nov/Dec 2016)
12. List the non-ideal DC characteristics of an OP-AMP. (Nov/Dec 2016)

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. The op-amp is configured as an inverting amplifier with R_1=1kΩ and R_f = 10kΩ. Calculate exact closed loop gain, ideal closed loop gain and compare these two results. (March 2016)
2. Draw the differential amplifier circuit using op-amp and explain its working. (March 2016)
3. Design a subtractor circuit whose output is equal to the difference between the two inputs. Use a basic differential op-amp configuration. (March 2016)
4. Design a subtractor circuit whose output is equal to the difference between the two inputs. Use a basic differential op-amp configuration. (March 2016)
5. Explain the four Differential Amplifier configurations. (March 2017)
6. Classify IC s and write about the Chip size. (Nov/Dec 2017)
7. Derive input resistance for inverting amplifier with feedback arrangement. (Nov/Dec 2017)
8. What is the operation performed by an inverting Op-Amp amplifier if its feedback resistance is replaced by a capacitance? Explain the functioning of such circuit. What are the practical difficulties associated with this circuit? (Nov/Dec 2017)
9. An IC op-amp 741 used as an inverting amplifier with a gain of 100. The voltage gain vs frequency characteristic is flat up to 12 kHz. Find the maximum peak to peak input signal that can be feed without causing any distortion to the output. (Nov/Dec 2017)
10. Derive input resistance for inverting amplifier with feedback arrangement. (Nov/Dec 2016)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. The effect of $I_{B\,is}$ _____ I_{io} on the o/p offset voltage [ ]
   a) less than b) greater than c) equal to d) None

2. AC characteristics of an OP-amp are _____ [ ]
   a) offsetcurrentb) offset voltage c) ($1+ R_1 / R_F$) d) slew rate

3. The closed loop gain of a non-inverting amplifier is [ ]
   a) ($1+ R_F/R_1$) b) R_F/R_1 c) ($1+ R_1 / R_F$) d) $-R_1 / R_F$

4. In a voltage follower the [ ]
   a. Non inverting input is shorted to output
   b. Inverting input is shorted to output.
   c. Both inputs are shorted to output
   d. None of the above

5. CMRR is defined as [ ]
   a. A_{DM}/A_{CM} b. A_{CM}/A_{DM}
   c. $(A_{CM} + A_{DM})/ ADM$ d. $A_{DM}/(A_{CM}+A_{DM})$

6. In which of the following integration number of gates available are 300 to 3000 per chip [ ]
   a) SSI b) MSI c) LSI d) VLSI

7. In ideal Op- amp the input impedance is [ ]
   a) $R_i = 0$ b) $R_i = 1$ c) $R_i = \infty$ d)none

8. Which of the following is First stage of Op-amp Internal circuit [ ]
   a) Buffer amplifier b) CB amplifier c) A pair of differential amplifier d) o/p driver

9. Which of the following is the closed loop gain of Non inverting amplifier [ ]
   a) $(1 + R_1/R_F)$ b) $(1 – R_F/R_1)$ c) $- R_F/R_1$ d) $(1 + R_F/R_1)$

10. Small difference between I_B+ and I_B- at the I/P of Op-amp circuit is known as [ ]
    a) Bias difference b) I/P OFF set current c) O/P OFF set current d) none
11. At higher frequencies gain of practical Op-amp will [ ]
    a) Increase b) Decrease c) Moderate d) None

12. For sine wave I/P slew rate [ ]
    a) $2\Pi V_m$ v/s b) $2\Pi f V_m$ v/s c) f / V_m s/v d)None

13. Which of the following are applications of 741-Op-amp [ ]
    a)Voltage follower b) Integrator c) Summer d)All the above

14. In an Inverting amplifier if gain = -10 and I/P resistance = 10Kohms [ ]
    then R_F =
    a) 1Kohm b)10^5 ohm c) 10Kohm d) 3Kohm

15. If R_1= 10kohm and R_F = 40 kohms , then the gain of non inverting amplifier is
    a) –10 b) +10 c) –5 d)5 [ ]
16. The differential amplifier can also be used as _____ckt [ ]
    a) Adder b) Subtractor c)Multiplier d) divider

17. choose the limitation of an integrated circuit [ ]
    a) Less weight b) Less heat dissipation c) Less cost d) Less power consumption

18. The output of an analog IC is a _____ [ ]
    a) Linear function b) exponential function c) Non-linear function d) trigonometric function

19. The Common mode output of a differential amplifier with a differential mode gain of 400 and CMRR of 80dB and a common mode input of $4\sin 200\pi t$ V is [ ]
    a) $0.5\sin 200\pi t$ b) $1.2\sin 200\pi t$ c) $0.16\sin 200\pi t$ d) $0.2\sin 200\pi t$

20. The difference between the two input bias currents when the output voltage is zero is called _____

ANSWERS

1. b	2.d	3.a	4.b	5.a
6.C	7.C	8.C	9.d	10.b
11.a	12.b	13.d	14.b	15.d
16.b	17.b	18.a	19.c	20. Input offset voltage

Unit-II: Op-amp and Applications:

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

1. High common mode voltage range make the μA741 ideal for use as voltage follower.
2. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications.
3. 741 is available in all 3 packages viz 8-pin metal can, 10-pin flat pack, and 8 or 14 pin DIP.
4. Basically there are 2 modes of op-amp. They are – Inverting Amplifier
   Non-Inverting Amplifier
5. APPLICATIONS OF OP-AMP
   Scale changer/Inverter.
   Summing Amplifier.
   Inverting summing amplifier
   Non-Inverting summing amplifier.
   Subtractor
   Adder
6. The input voltage is applied to the non-inverting input terminal and the feedback voltage across R drives the inverting input terminal. This circuit is also called a current series negative feedback, amplifier.
7. The sample and hold circuit, as its name implies samples an i/p signal and holds on to it last sampled value until the i/p is sampled again.
8. A circuit in which the output voltage waveform is the differentiation of input voltage is called differentiator.
9. A circuit in which the output voltage waveform is the integral of the input voltage waveform is called integrator.
10. Voltage comparator is a circuit which compares two voltages and switches the output to either high or low state depending upon which voltage is higher.
11. In non inverting comparator the reference voltage is applied to the inverting input and the voltage to be compared is applied to the non inverting input.
12. An inverting comparator with +ve feed back. This circuit converts an irregular shaped wave forms to a square wave form or pulse. The circuit is known as schmitt trigger or squaring circuit.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. What is the necessity of a sample & hold circuit? (March 2017)
2. What do you mean by voltage regulator? Discuss the types in it. (November – 2015)
3. List the features of 741 OP-AMP. (Nov/Dec 2016)
4. List out the ideal characteristics of op-amp. (Nov/Dec 2017)
5. Write the features of 741 op-amp. (Nov/Dec 2017)
6. List out the ideal characteristics of op-amp. (Nov/Dec 2017)
7. Define Input and Output Offset-voltages. (Nov/Dec 2018)
8. Compare Open loop and Closed loop configurations of Op-Amp. (Nov/Dec 2018)
9. Discuss how a voltage follower is built using an op-amp. (Nov/Dec 2016)
10. What is instrumentation amplifier? (Nov/Dec 2016)

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw the differential amplifier circuit using op-amp and explain its working. (March 2016)
2. Draw the circuit diagram of an Instrumentation amplifier and explain its working. (March 2016)
3. Explain the role of Low pass filter and VCO in PLL. (March 2016)
4. How PLL is used for frequency multiplier? Explain. (March 2016)
5. The input signal to an op-amp is $0.03 \sin 1.5 \times 10^5 t$. What can be the maximum Gain of an Op-Amp with the slew rate of 0.4 V / μsec? (March 2017)
6. Explain how a Multiplier can be used as a voltage divider. (March 2017)
7. Explain how the op amp is use as I-V converter. (November – 2015)
8. Explain and draw the output waveforms of the ideal integrator circuit when the input is i) sine wave ii) square wave and iii) step input. (November – 2015)
9. Design a op amp circuit which can give the output as $V_0 = 2V_1 - 3V_2 + 4V_3 - 5V_4$. (November – 2015)
10. Explain the operation of V to I converter. (Nov/Dec 2017)
11. Draw the circuit and explain the operation of Instrumentation Amplifier. Derive the expression for its output voltage. (Nov/Dec 2018)
12. An Op-Amp has a differential gain of 80 dB and CMRR of 95 dB. If $V_1 = 2$ μV and $V_2 = 1.6$ μV, then calculate differential and common mode output values. (Nov/Dec 2018)
13. Explain the principle of operation of Sample and Hold circuit. (Nov/Dec 2018)
6. What is instrumentation amplifier? What are the features of it? Explain any three applications of instrumentation amplifier. (Nov/Dec 2016)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1. At higher frequencies ____of op-amp limits the slope of the output square wave. [ ]
   a) gain b)slew rate c) output impedance d)None

2. The need of R_f in shunt with feed back capacitor C_f in the integrator ckt is [ ]
   a) To decrease low frequency gain b) To decrease o/p voltage variation c) To increase low frequency gain d) a & b

3. Which of the following is the application of the comparator [ ]
   1. Phase meter b) Window detector c) zero crossing detector d) All the above

4. Non-inverting amplifier is converted to voltage follower by making R_F =…. and R_1= ….. [ ]
   a)0,0 b)0,∝ c)∝,0 d)∝,∝

5. Which of the following is the zero DB frequency of the practical differentiator ckt [ ]
   a) $2\Pi R_f C_1$ b) $2\Pi R_f C_f$ c) $1 / 2\Pi R_f C_1$ d) $1 / 2\Pi R_f C_f$

6. Which of the following is the o/p waveform of the differentiator when a sinusoidal is passed through it [ ]
   a) spikes b) sine wave with 90^0 phase shift c) sine wave with 270^0 phase shift d) sine wave with no phase shift

7. Which of the following ckt is used to compress the dynamic range of the signal [ ]
   a) Comparator b) Inverting amplifier C)log amplifier d) Sample-Hold ckt

8 Which of the following ckt is used in pulse code modulation [ ]
a) log amplifier b) comparator ckt c) Sample & Hold ckt d) none

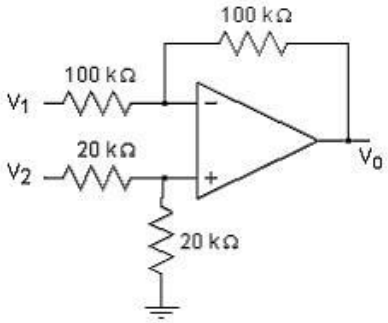
9 The phase angle between two voltages can also be measured using _____ circuit

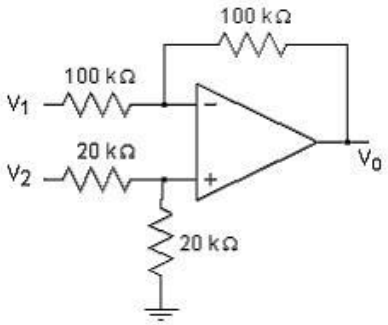
10 Write an expression for output voltage of an ideal integrator----------

11 The time taken for the op-amp output voltage to go from -10V to +10V with a slew rate of 0.5v/μs is [ ]
a)20μs b)30μs C) 40μs d)24μs

12. The output of an inverting amplifier with respect to input is [ ]
a) 180° out of phase b) 180° in-phase c) - 180° out of phase d) -180° in-phase

13 Determine the output voltage when $V1 = V2 = 1V$. [ ]

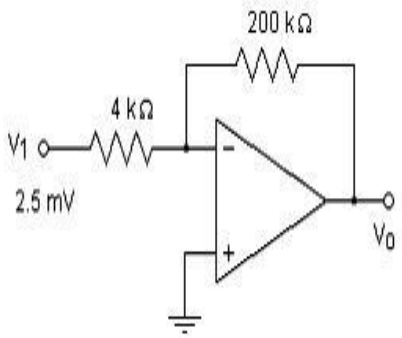




A)0 V B) –2 V C) 1 V D) 2 V

14. The overall voltage gain of an inverting amplifier, if $R1 = 100\ \Omega$ and $Rf = 1\ k\Omega$ [ ]
a) -1 b) 10 c) 11 d) 9

15. The output of a cascaded differential amplifier is_____
16. In the absence of input voltage or at zero frequency (d.c),op-amp gain is _____
17. Determine the output voltage for this circuit with a sinusoidal input of 2.5 mV.



V_0= ____

18. In voltage-to-current converter the output load current is____
19. In an integrator circuit if input is step, output is ____
20. A triangular square-wave generator uses_____

ANSWERS:

1. b	2.d	3.d	4.b	5.c
6.b	7. c	8.c	9.Multiplier	10.V_O=-1/$R_1C_F\int V_i$
11.c	12.a	13.a	14.b	15. Unbalanced output
16. very high	17. -0.125V	18.proportional to the input voltage	19.ramp	20.Integrator&comparator

Unit-III: Active Filters & Oscillators

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

1. An electric filter is often a frequency-selective circuit that passes a specified band of frequencies and blocks or attenuates signals of frequencies outside this band. Filters may be classified in a number of ways: 1. Analog or digital 2. Passive or active 3. Audio (AF) or radio frequency (RF)
2. First-order low-pass Butterworth filter that uses an RC network for filtering.
3. A band-pass filter has a pass band between two cutoff frequencies fH and fL such that fH>fL. Any input frequency outside this pass band is attenuated. Basically, there are two types of band-pass filters: (1) Wide band pass, and (2) Narrow band pass.
4. A wide band-pass filter can be formed by simply cascading high-pass and low-pass sections and is generally the choice for simplicity of design and performance.
5. The narrow band-pass filter using multiple feedback , the filter uses only one op-amp. Compared to all the filters, this filter is unique in the following respects 1. It has two feedback paths, hence the name multiple-feedback filter. 2. The op-amp is used in the inverting mode.
6. The band-reject filter is also called a band-stop or bandelimination filter. In this filter, frequencies are attenuated in the stop band while they are passed outside this band.
7. The band-reject filters can also be classified as (1) wideband-reject or (2)narrowband-reject.
8. The narrow band-reject filter is commonly called the notch filter. Because of its higher Q (>10), the bandwidth of the narrow band-reject filter is much smaller than that of the wideband- reject filter.

9. An all-pass filter passes all frequency components of the input signal without attenuation, while providing predictable phase shifts for different.
10. The function of an oscillator is to generate alternating current or voltage waveforms.
11. An oscillator is a circuit that generates are petitive waveform of fixed amplitude and frequency without an y external input signal.
12. Oscillators are used in radio, television, computers, and communications.
13. The difference between the triangular and sawtooth waveforms is that the rise-time of the triangular wave is always equal to its fall-time. That is, the same amount of time is required for the triangular wave to swing from –Vramp to +Vramp as from +Vramp to-Vramp.
14. The sawtooth waveform has unequal rise and fall times.
15. Where the frequency needs to be controlled by means of an input voltage called controlled voltage. This function is achieved in the voltage controlled oscillator (VCO) also called a voltage to frequency converter.
16. A typical example is the signetics NERSE 566 VCO, which provides simultaneous square wave and triangular wave outputs as a function of input voltage.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. What are the advantages of active filters? (March 2016)
2. What is VCO? Discuss. (March 2016)
3. List different types of Filters. (March 2017)
4. State the Barkhausen criterion. (March 2017)
5. Design a notch filter to eliminate 120Hz signal. (November – 2015)
6. What are the advantages of active filter over passive filter? (November – 2015)
7. Mention the differences between band pass and Band Reject filter. (Nov/Dec 2017)
8. What is the use of VCO? (Nov/Dec 2018)
9. Compare 1st order Low Pass and High Pass filters. (Nov/Dec 2018)
7. What is an Active filter? What are the advantages offered by it over a passive filter? (Nov/Dec 2016)

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Design a second order High pass active filter with cutoff frequency of 2 kHz and also draw its frequency response. (March 2016)
2. Draw the circuit diagram of quadrature oscillator and derive the equation for frequency of oscillations and also design such a circuit to generate oscillations at a frequency of 159 Hz. (March 2016)
3. Draw the functional block diagram of 555 timer and explain its operation. (March 2016)
4. What are the applications of 555 timer and explain any one application in detail. (March 2016)
5. Discuss the amplitude stabilization of Phase shift Oscillator. (March 2017)
6. Design and draw the circuit diagram of a Wein bridge Oscillator using op-amp to produce sustained oscillations of a time period of 0.1 m sec. (March 2017)
7. Obtain the Transfer function of the first order High pass Butter worth filter. (March 2017)
8. Design a phase shift oscillator to have output frequency of 500Hz. Use ±12V supply. (November – 2015)
9. Draw and analyze the second order low pass Butterworth filter. (November – 2015)
10. Explain with the help of the neat diagram and waveforms working of triangular wave generator. (November – 2015)
11. Discuss the applications of VCO. (November – 2015)
12. Derive the expression for the transfer function of first order high pass filter. (Nov/Dec 2017)
13. Draw the schematic diagram of Wein bridge oscillator and explain its working.
14. Explain the operation of VCO. (Nov/Dec 2017)
15. Discuss about the operation of Wein Bridge Oscillator. (Nov/Dec 2017)

16. Draw the basic circuit of RC - Phase Shift Oscillator and explain its operation. Also derive the expression for frequency of Oscillation. (Nov/Dec 2018)
17. Design first order high pass filter with a cut off frequency of 10 KHz with a pass band gain of 1.5. (Nov/Dec 2018)
18. Explain various types of filters along with their frequency response. (Nov/Dec 2018)
19. In an AC inverting amplifier circuit R_{in}=50Ω, C_i= 0.1μF, R_1=100KΩ, R_f=1KΩ, R_2=10KΩ and V_{cc}=±15V. Determine the Bandwidth of the amplifier. (Nov/Dec 2016)
20. Design a first order active high pass filter with cutoff frequency of 2KHz with op-amp. Why this is called Active filter? (Nov/Dec 2016)
21. Design a Triangular wave generator with f_0= 1.5 KHz andV_0 (PP) = 5V. 6.a) Derive the expression for the transfer function of first order high pass filter. (Nov/Dec 2016)
22. Draw the schematic diagram of Wein bridge oscillator and explain its working. (Nov/Dec 2016)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1 To realize butter-worth 3rd order filter one can combine …. order and ….. order filters [ ]
a) 1 & 2 b) 5 & 2 c) 4 & 1 d) none

2 A HPF will [ ]
a) Pass high frequencies b) Pass low frequencies c) Block DC d) a & c

3 With the increase in order of the filter, the gain will increase or decrease at the rate of [ ]
a) 40 dB/decade b) 60 dB/Decade c) 20 dB/Decade d) none

4 ……..filter is used to reject an unwanted frequency like 50 HZ

5 For sustained oscillation, how many conditions must be satisfied [ ]
a) 4 b)3 c) 2 d) 1

6 Which of the following are elements of passive filters [ ]
a)op-amps b)R,L,C c)diode D) Transistors

7 In which of the following range of frequencies are attenuated [ ]
a) stop band b)pass band c)band pass d)none

8 Which of the following filter is also called as Multiple feedback filter [ ]
a) Wide band pass filter b) Narrow band pass filter c) wide band elimination filter d) Narrow band elimination filter

9 A low pass filter will [ ]
a)Pass high frequencies b)Block low frequencies c)pass DC d) Block DC

10 . A high pass filter [ ]
a) pass high frequencies b)pass low frequencies c) pass DC d)none

11 Above cutoff frequency of 4th order LPF output voltage decrement rate of [ ]
a) 20db/decade b)40db/decade c) 60db/decade d) 80db/decade

12 Below cutoff frequency of 2nd order HPF the output voltage increase at a rate of [ ]
a) 20db/decade b) 40db/decade c) 60db/decade d) 80db/decade

13 All pass filter is also called as…… [ ]
a) Delay equalizers b) Phase correctors c) Notch filter d) a & b

14 Butter worth filter response have a ……. pass band &……..stop band
a) Flat, Flat b) Ripple , Ripple c) Flat, Ripple d) Ripple, Flat

15 Combine…….order&……order filters
a)1&2 b)5&2 c)4&1 d)none

16 Standard transfer function of narrow band reject filter is given by ……. [ ]
a) $\frac{-A_0(S^2+\omega^2)}{S^2+\alpha\omega_0 S+\omega_0^2}$ b) $\frac{A_0}{S^2+\alpha\omega_0 S+\omega_0^2}$ c) $\frac{A_0(S^2+\omega^2)}{S^2+\alpha\omega_0 S+\omega_0^2}$ d) $\frac{\omega^2}{S^2+\alpha\omega_0 S+\omega_0^2}$

17 Below the cut off frequency of fourth order of HPF the output voltage decreases at a rate of _____ db/decade
a) 20 b) 40 c) 60 d) 80

18 Which of the following is called Relaxation oscillator. [ ]
a) Colpitts b) Hartley c d c) Saw tooth wave generator d)RC Phase shift

19 Narrow band reject filter is commonly called as ……. Filter

20 The frequency at which maximum attenuation occurs in notch filter is called as _____

21 A band pass response has [ ]
a) 2-critical frequencies b) 1-critical frequency c) A flat curve in the pass band d) A wide bandwidth

22 The frequency of Wien bridge oscillator is decided by

23 A first-order low-pass Butterworth filter is realized by a RC network and _____

ANSWERS:

1.a	2.d	3.c	4.LPF	5.c
6.b	7.a	8.a	9.c	10.a
11.d	12.b	13.d	14.a	15.a
16.c	17.d	18.d	19.Narrow band elimination	20.cut-off
21.a	22. series RC network	23. a non-inverting amplifier		

Unit-IV: Timers & Phase Locked Loops:

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

1. One of the most versatile linear integrated circuits is the 555 timer.
2. A sample of these applications includes mono-stable and astable multivibrators, dc-dc converters, digital logic probes, waveform generators, analog frequency meters and tachometers, temperature measurement and control, infrared transmitters, burglar and toxic gas alarms, voltage regulators, electric eyes, and many others.
3. A monostable multivibrator, often called a one-shot multivibrator, is a pulse-generating circuit in which the duration of the pulse is determined by the RC network connected externally to the 555 timer.
4. The monostable multivibrator can be used as a frequency divider by adjusting the length of the timing cycle tp, with respect to the tine period T of the trigger input signal applied to pin 2.
5. To use monostable multivibrator as a divide-by-2 circuit, the timing interval tp must be slightly larger than the time period T of the trigger input signal.
6. Pulse stretcher: This application makes use of the fact that the output pulse width (timing interval) of the rnonostable multivibrator is of longer duration than the negative pulse width of the input trigger.
7. An Astable Multivibrator, often called a freerunning multivibrator, is a rectangular- wave-generating circuit.
8. The phase-locked loop principle has been used in applications such as FM (frequency modulation) stereo decoders, motor speed controls, tracking filters, frequency synthesized transmitters and receivers, FM demodulators, frequency shift keying (FSK) decoders, and a generation of local oscillator frequencies in TV and in FM tuners.
9. The phase-locked loop is even available as a single package, typical examples of which include the Signetics SE/NE 560 series (the 560, 561, 562, 564, 565, and 567).
10. The phase detector compares the input frequency and the VCO frequency and generates a dc voltage that is proportional to the phase difference between the two frequencies.
11. Monolithic PLLs are introduced by signetics as SE/NE 560 series and by national semiconductors LM 560 series.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. What are the basic building blocks of PLL? (March 2016)
2. What are the basic differences between the two operating modes of the 555 timer? (March 2016)
3. Mention the applications of the Schmitt trigger. (March 2017)
4. What is the importance of Pin 5 of IC 555? (March 2017)
5. What are the features of 555 timers? (November – 2015)
6. Explain the importance of control voltage pin 5 of the timer 555. (November – 2015)
7. Mention the blocks present in IC565. (Nov/Dec 2017)
8. What are the modes of operation of a Timer? (Nov/Dec 2017)
9. List various applications of IC 555 Timer. (Nov/Dec 2017)
10. Draw the block diagram for PLL. (Nov/Dec 2018)
11. Distinguish between Astable and Monostable Multi-vibrators. (Nov/Dec 2018)
12. What are the modes of operation of a Timer? (Nov/Dec 2016)
13. What is the major difference between digital and analog PLLs? And list the applications of PLL. (Nov/Dec 2016)

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. Draw the functional block diagram of 555 timer and explain its operation. (March 2016)
2. What are the applications of 555 timer and explain any one application in detail. (March 2016)
3. Explain the role of Low pass filter and VCO in PLL. (March 2016)
4. How PLL is used for frequency multiplier? (March 2017)
5. Draw the circuit and explain how IC555 can be used for Pulse Position Modulation (PPM). (March 2017)
6. Explain the functioning of 555 in Monostable configuration. (March 2017)
7. Describe any four applications of Phase Locked Loop with the help of suitable circuit diagrams. (March 2017)
8. Design a 555 based square wave generator to produce a symmetrical square wave of
9. 1KHz. If V_{CC}=12V draw the voltage across timing capacitor and the output. (November – 2015)
10. Give the applications of Astable multivibrator. (November – 2015)
11. Derive the Lock range and capture range in PLL. (November – 2015)
12. Explain the PLL as a FM detector. (November – 2015)
13. Describe the functional block diagram of 555 timer. (Nov/Dec 2017)
14. How 555 timer can be used in Schmitt Trigger circuit. (Nov/Dec 2017)
15. With a neat diagram explain the operation of PLL. (Nov/Dec 2017)
16. Write about the applications of PLL. (Nov/Dec 2017)
17. Derive the expression for the Duty cycle of an Astable Multi-vibrator using IC555. (Nov/Dec 2018)
    Compare and contrast Schmitt trigger and Comparator. (Nov/Dec 2018)
    Derive an expression for Capture Range of PLL. (Nov/Dec 2018)
    Show that the Lock-in Range of a PLL is given by $Af_L = \pm 7.8f_o/V$, Where the symbols used have the usual meaning. (Nov/Dec 2018)
18. Describe the 555 timer monostable multivibrator applications in pulse stretching. (Nov/Dec 2016)
    Design a 555 timer circuit whose output frequency is 2KHz when the trigger input signal frequency is KHz. (Nov/Dec 2016)
19. Explain the operation of frequency multiplier using PLL. (Nov/Dec 2016)
20. Define Lock-in range, Capture range and Pull-in time in PLL system. (Nov/Dec 2016)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1 Which of the following is the feature of 555 timer [ ]
a) Adjustable duty cycle b) It provides time delay c) It is compatible with TTL and CMOS circuit d) All the above

2 Which of the following is dual timer IC [ ]
a)IC 555 b) IC 565 c) IC 556 d)IC 1496

3 Which of the following is Balanced modulator [ ]
a)IC 556 b)IC565 C)IC1496 d)IC 555

4 Which of the following IC works as phase locked loop [ ]
a)IC 556 b)IC 565 d)IC 555 c)IC 1596

5 Which of the following can be used as both linear & switched regulator [ ]

a)IC 555 b)IC 7805 c)IC 7912 d) IC 723

6 In which of following regulator ,Transistor will act as a controlled switch [ ]
a) Regulated power supply b)SMPS c) IC 7809 d) 7905

7 .----------circuit can be also called as square wave converter [ ]
a) Bi stable multi vibrator b)Mono stable multi vibrator c)A stable multi vibrator d)Schmitt trigger

8 A stable multi vibrator is also called as [ ]

a)Square wave converter b)Square wave generator c)Sine wave generator d)Triangular wave generator

9 Which of the following is the expression for pulse width of 555 mono stable multivibrator
a)1.1 $R_A C$ b)0.69 RC c)0.119RC d)none

10 Free running frequency of 565 PLL is [ ]
a) $0.3/ R_1 C_1$ b) $1.2/ R_1 C_1$ c) $1.45/ R_1 C_1$ d)$2.2 R_1 C_1$

11 Which of the following is an application of 555 IC Astable [ ]
a) PWM generator b) PPM generator c) FSK demodulator

12 To use Monostable multivibratror as divide –by-2 circuit the relation between the length of timing cycle t_p and the time period of the trigger input T is [ ]

13. What does the discharge transistor do in the 555 timer circuit? [ ]
A) charge the external capacitor to stop the timing
B) charge the external capacitor to start the timing over again
C) discharge the external capacitor to stop the timing
D) discharge the external capacitor to start the timing over again

14. The Control voltage in a VCO is also called [ ]
A)Difference input voltage B) Operating input voltage
C) Modulating input voltage D) Capacitor input voltage

15. A monostable 555 timer has the _____ number of stable states

16. Three configurations for switching regulators are _____
17. Timing range of 555 timer is_____
18.Capacitor charged on a monostable multivibrator (IC 555)_____
19.Astable multivibrator (555 timer) generates a frequency for unsymmetrial square wave_____
20.The lock range is usually _____than the capture range.

ANSWERS:

1.d	2.b	3.c	4.b	5.d	6.c
7.d	8.b	9.b	10.d	11.c	12.c
13.d	14.c	15.1	16. step-down,step-up&inverter	17.micro seconds to ho	18.(1/3)V_{CC}
19.1.45/(R_A+R_B)C	20. >				

Unit-V: D-A and A-D Converters:

Important points / Definitions: (Minimum 15 to 20 points covering complete topics in that unit)

1. An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integrating type A/D converter
2. Wide range of resistors required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC.
3. In weighted resistor and R-2R ladder DAC the current flowing through the resistor is always changed because of the changing input binary bits 0 and 1. More power dissipation causes heating, which in turn cerates non-linearity in DAC. This problem can be avoided by using INVERTED R-2R LADDER DAC.
4. A direct-conversion ADC or flash ADC has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range
5. One method of addressing the digital ramp ADC's shortcomings is the so-called successive-approximation ADC.
6. A successive-approximation ADC uses a comparator to reject ranges of voltages, eventually settling on a final voltage range. Successive approximation works by constantly comparing the input voltage to the output of an internal digital to analog converter.
7. The Resolution of a converter is the smallest change in voltage which may be produced at the output of the converter.
8. Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
9. The most important dynamic parameter is the settling time. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input.
10. The performance of converter changes with temperature, age and power supply variations.

Short Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. What is the advantage of R-2R ladder D/A converter over the one with binary weighted resistors? (March 2016)
2. What are the different types of ADCs and compare them in terms of speed of operation. (March 2016)
3. List the various A/D conversion techniques. (March 2017)
4. List the draw backs of Binary weighted Resistor technique D/A conversion. (March 2017)
5. An 8 bit successive approximation type ADC is driven by a 1MHz clock. Find the conversion time. (November – 2015)
6. What are the different sources of errors in DAC? (November – 2015)
7. Explain how Dual-slope ADC provides noise rejection? (Nov/Dec 2017)
8. Compare R-2R and Weight Resistor types of ADC. (Nov/Dec 2017)
9. Which is the fastest ADC and why? (Nov/Dec 2018)
10. For a particular 8-bit ADC, the conversion time is 9 μs. Find the maximum frequency of an input sine wave that can be digitized. (Nov/Dec 2018)
11. How many resistors are required in a 12-bit weighted resistor DAC? Why? [2]
12. Explain how Dual-slope ADC provides noise rejection?

Long Questions (minimum 10 previous JNTUH Questions – Year to be mentioned)

1. For the D/A converter using an R-2R ladder network, determine the size of each step if
2. $R_f = 27k\Omega$ and $R = 10k\Omega$ and also calculate the output voltage when the inputs b_0, b_1, b_2 and b_3 are at 5V. (March 2016)
3. Draw the circuit diagram of binary-weighted resistor DAC and explain its working. (March 2016)
4. Draw the circuit diagram of Dual slope ADC and explain its working. (March 2016)
5. What is the role of DAC in successive approximation ADC? (March 2016)
6. Describe Parallel Comparator type ADC operation. (March 2017)
7. Explain the working of Inverted R-2R ladder D/A converter. (March 2017)
8. Find out the Step size and Analog output when input is 0011 and 1011. Assume $V_{ref} = +5V$. (March 2017)
9. Explain Successive Approximation ADC with the help of block diagram. (March 2017)
10. Explain the working of weighted resistor D/A converter and state its features. (November – 2015)
11. Find the resolution of a 12 bit D/A converter. (November – 2015)
12. Explain the working of dual slope A/D converter. (November – 2015)
13. Draw the IC 1408 DAC pin diagram and explain. (November – 2015)
14. Explain the operation of Successive approximation ADC. (Nov/Dec 2017)
15. Write about the ADC specifications. (Nov/Dec 2017)
16. Discuss about the binary weighted resistor DAC. (Nov/Dec 2017)
17. Mention the applications of DAC and ADC. (Nov/Dec 2017)
18. Find the Resolution of 12-bit D/A Converter. (Nov/Dec 2018)
19. An 8-bit Successive Approximation ADC is driven by a 1 MHz clock. Find its Conversion time. (Nov/Dec 2018)
20. Obtain an expression for the output voltage of R-2R DAC. (Nov/Dec 2018)
21. Explain how Dual Slope A/D converter provides Noise rejection. (Nov/Dec 2018)
22. Compare the dual slope ADC with successive approximation ADC. (Nov/Dec 2016)
23. Explain the operation of R-2R ladder DAC with the help of neat diagrams. (Nov/Dec 2016)
24. Explain the operation of flash ADC using relevant diagrams. (Nov/Dec 2016)
25. What are the merits and demerits of counter type ADC? Explain. (Nov/Dec 2016)

Fill in the Blanks / Choose the Best: (Minimum 10 to 15 with Answers)

1 Feed Through Rejection Ratio is computed as [ ]
2 Arrange the following ADC's in the order of speed – fastest on top slowest below
3 A 12 bit DAC has a reference voltage of 5.0 V. What is its resolution in mVolts.----------

4 Depending upon the conversion technique , ADC's are classified as …….. and ……..…

5. ---------- DAC uses many different values of resistors

6. ---------- DAC uses only two different values of resistors.

7. The Inverted R-2R DAC is better than R-2R DAC because ----------

8. The Part Number of one of the Monolithic DAC is _____

9. The Inverted R-2R DAC is better than R-2R DAC because ----------

10. The Part Number of one of the Monolithic DAC is _____

11. Name the two classes of Analog to Digital Convertors----------

12. The control Signals of an ADC are----------
13. Weighted Resistor DAC makes use of _____voltage [ ]
a) –Ve reference b) +Ve reference c) 0 reference d) double

14. In the digital domain a signal is represented as a series of numbers (low/high/logic levels) [ ]
a) flexibility b) repeatability c) long-term storage d) cost

15. _____is also defined as tha ratio of a change in value of input voltage Vi, needed to change the digital output by 1 LSB. If the full scale input voltage required cause a digital output of all 1s is V.

16. Number of comparators preferred in 3-bit ADC is _____

17. Conversion time of successive approximation ADC for n-bit is _____

ANSWERS:

1.a	2.b	3.C	4.B	5.D	6.c
7. a	8.b	9.c	10.d	11.a	12.b
13.a	14.b	15.Resolution	16.8	17. T(n+1)	